ABC IT
FOR AUTOMATION

User Manual

ABC-CPU Systems

Parameterization

15/2012

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1. Parametrisation

1.1 General

The parameterisation possibilities of the CPU software S7/S5 for the X-CPU-6 are described in the following.

The X-CPU-6 S5 software CPU945 and CPU948 are principally parameterised by way of the DB1 and DX1 of the respective CPU type.

The X-CPU-6 S7 software CPU416, CPU416/948 and CPU416/945 are parameterised by way of the HW configuration of the Simatic Manager, as well as by way of a SYSPARAM DB to be defined.

The parameterisation is identical for all supported operating systems. However, depending upon the operating system and hardware adaption, not all parameters are supported.

1.2 ABC X-CPU-6 CPU945

The X-CPU-6 CPU945 software is parameterised by way of the DB1 and DX1. These components are contained in the CPU following overall reset and can be adapted in accordance with requirements.

```
"DB1                        "
"# System-Dependent         "
"---------------------- # "
"SDP:                       "
"WD 500                     "
"RT 64                      "
"RC 64                      "
"RF 128                     "
"RS 2048                    "
"PROT N                     "
"PIO N                      "
"PII N                      "
";                          "
"# Timer-Function-Block"
"---------------------- # "
"TFB:                       "
"OB13 100                   "
";                          "
"END                        ";
```

DB1 template following overall reset of the CPU with default settings

SDP	
WD t	Cycle monitoring time
RDLY t	RUN delay in ms
PROT N/Y	Protection Flag
PIO N/Y	The process image of the outputs is blocked/ is cyclically processed
PII N/Y	The process image of the inputs is blocked/ is cyclically processed
RT n, N, Y	n remanent timer, N no timer remanent, Y 64 timer remanent
RC n, N, Y	n remanent counter, N no counter remanent, Y 64 counter remanent
RF n, N, Y	n remanent marker, N no marker/SMarker remanent, Y 128 marker, 2048 SMarker remanent
RS n, N, Y	n remanent SMarker, N no SMarker remanent, Y 2048 SMarker remanent

TFB	

OB10 n .. OB13 n	Wake-up alarms OB10 to OB13. The priority of the components in ascending order with: OB10 low prior to OB13 high prior. The time assignment can be individually parameterised in ms

```
"DX1                        "
"# System-Dependent         "
"---------------------- # "
"SDP:                       "
"MZ  0                      "
"TM -1                      "
";                          "
"# Inf.Tech. - Parameter "
"---------------------- # "
"ITP<0>:                    "
"INET 0.0.0.0               "
"MASK 0.0.0.0               "
"ROUT 0.0.0.0               "
"GUI  N                     "
"DHCP N                     "
"DNS  0.0.0.0               "
"HOST X5                    "
"DOM  ABCIT                 "
";                          "
"END                        ";
```

DX1 template following overall reset of the CPU

SDP	
MZ t	Minimum cycle time
TM n	Tact marker byte in the SMARKER area

ITP <x>	IP address of CP x define; ETH1==CP0,…ETH4==CP3
INET	IP address 192.168.0.90
MASK	Subnet mask 255.255.255.0
ROUT	Router address 192.168.0.1
DHCP	DHCP active Y/N
DNS	DNS server address 192.168.0.1
HOST	Host name “X7”
DOM	Domain name ‘ABCIT”
GUI	Graphical User Interface aktiv J/N

CIFX<0>	*Extensionboard*

D XX	Device DP=Profibus, PN=Profinet, EC=EtherCAT
BF N/Y	Bus-Fault Y/N
I x y	Input from offset x length y Byte
O x..y	Output from offset x length y Byte
PII x y	Process Image Inputs from offset x length y Byte
PIO x y	Process Image Output from offset x length y Byte

1.3 ABC X-CPU-6 CPU948

The RS5-948 CPU software is parameterised by way of the DB1 and DX1. These components are contained in the CPU following overall reset and can be adapted in accordance with requirements.

```
"DB1                        "
"# System-Dependent         "
"---------------------- # "
"SDP:                       "
"WD   500                   "
"RDLY 0                     "
"INT  O                     "
";                          "
"# Timer-Function-Block     "
"---------------------- # "
"TFB:                       "
"OB10 10                    "
"OB11 20                    "
"OB12 50                    "
"OB13 100                   "
"OB14 200                   "
"OB15 500                   "
"OB16 1000                  "
"OB17 2000                  "
"OB18 5000                  "
";                          "
"# Hardware process         "
   alarms                   "
"---------------------- # "
"INTX:                      "
"INTA N                     "
"INTE N                     "
"INTF N                     "
"INTG N                     "
";                          "
"# Process alarms EB0       "
"---------------------- # "
"PRAL:                      "
"EB0  Y                     "
";                          "
"# Priority assignment      "
"Range 2..28                "
"---------------------- # "
"PRIO:                      "
"OB1   2                    "
"OB2  19                    "
"OB3  18                    "
"OB4  17                    "
"OB5  16                    "
"OB6  15                    "
"OB7  14                    "
"OB8  13                    "
"OB9  12                    "
"OB10 28                    "
"OB11 27                    "
"OB12 26                    "
"OB13 25                    "
"OB14 24                    "
"OB15 23                    "
"OB16 22                    "
"OB17 21                    "
"OB18 20                    "
";                          "
"END                        ";
```

DB1 template following overall reset of the CPU

SDP	
WD t	Cycle monitoring time
RDLY t	RUN delay in ms
INT O/B	Interruption at O/C (Operations/component limits)
PROT N/Y	Protection Flag
PIO N/Y	The process image of the outputs is blocked/ is cyclically processed
PII N/Y	The process image of the inputs is blocked/ is cyclically processed
RT n, N, Y	n remanent timer, N no timer remanent, Y 64 timer remanent
RC n, N, Y	n remanent counter, N no counter remanent, Y 64 counter remanent
RF n, N, Y	n remanent marker, N no marker/SMarker remanent, Y 128 marker
RS n, N, Y	n remanent SMarker, N no SMarker remanent, Y 2048 SMarker remanent

TFB	
OB10 n .. OB18 n	Wake-up alarms OB10 to OB13. The priority of the components in ascending order with: OB10 low prior to OB13 high prior. The time assignment can be individually parameterised in ms

INTX	
INTA-D, E, F, G N/Y	The hardware process alarms depend upon the slot. A-D are represented by the CPU slots 1-4 in a 135/155 system. Attention: the EB0-PRAL must be deactivated when INTX is active.

PRAL	
EB0 Y/N	The EB0 process alarm recognises flank changes on the EB0 and triggers the accordingly assigned OBs: EB 0.0 → OB2 .. EB 0.7 → OB9 Attention: the INTX must be deactivated when EB0-PRAL is active.

PRIO	
OBn p	With the priority assignment it is possible to control the capacity for interruption of the individual components.

CIFX<0>	*Extensionboard*
D XX	Device DP=Profibus, PN=Profinet, EC=EtherCAT
BF N/Y	Bus-Fault Y/N
I x y	Input from offset x length y Byte
O x..y	Output from offset x length y Byte

PII x y	Process Image Inputs from offset x length y Byte
PIO x y	Process Image Output from offset x length y Byte

```
"DX1                        "
 "# System-Dependent         "
 "--------------------- # "
 "SDP:                       "
 "MZ  0                      "
 "TM -1                      "
 ";                          "
 "# Inf.Tech. - Parameter "
 "--------------------- # "
 "ITP<0>:                    "
 "INET 0.0.0.0               "
 "MASK 0.0.0.0               "
 "ROUT 0.0.0.0               "
 "GUI  N                     "
 "DHCP N                     "
 "DNS  0.0.0.0               "
 "HOST X5                    "
 "DOM  ABCIT                 "
 ";                          "
 "END                        ";
```

DX1 template following overall reset of the CPU

SDP	
MZ t	Minimum cycle time
TM n	Tact marker byte in the SMERKER area

ITP <x>	IP address of CP x define; ETH1==CP0,…ETH4==CP3
INET	IP address 192.168.0.90
MASK	Subnet-Mask 255.255.255.0
ROUT	Router Address 192.168.0.1
DHCP	DHCP active Y/N
DNS	DNS server address 192.168.0.1
HOST	Host name “X7”
DOM	Domain name ‘ABCIT”
GUI	Graphical User Interface aktiv J/N

CIFX<0>	*Extensionboard*
D XX	Device DP=Profibus, PN=Profinet, EC=EtherCAT
BF N/Y	Bus-Fault Y/N
I x y	Input from offset x length y Byte
O x..y	Output from offset x length y Byte
PII x y	Process Image Inputs from offset x length y Byte
PIO x y	Process Image Output from offset x length y Byte

1.4 ABC X-CPU-6 CPU416, CPU416/945, CPU416/948

The X-CPU-6 CPU416 software can be parameterised as follows:

- Default settings
- Start parameters and default IP addresses (cmdline.txt on the SD card)
- HW configuration of the Simatic Manager
- SYSPARAM data component

The diverse settings of the X-CPU-6 CPU416 software are not completely covered by the possibilities of the HW configuration of the Simatic Manager. Supplements / expansions can thus only take place via the SYSPARAM data component.

The sequence of parameterisation is defined as follows:

1) The default settings are loaded
2) Settings made in the SYSPARAM data component replace the default settings.
3) Settings carried out in the HW configuration of the Simatic Manager replace the currently valid values.

Note

The parameterisation also applies to the X-CPU-6 CPU416/945 and CPU416/948 software. In this case, the DB1 and DX1 in the S5 part have no significance.

1.4.1 Start parameters and default IP addresses (cmdline.txt)

IMPORTANT!!! Before the SD card on the X-CPU-6 is removed, the module must be de-energised and a waiting period should be observed until no LED at the front lights any longer.

The file cmdline.txt is stored on the SD card in the folder rs7.

Various start parameters can be defined in this file. The default IP addresses are first accepted following the overall reset and a STOP□RUN transition.

The cmdline.txt is structured as follows:

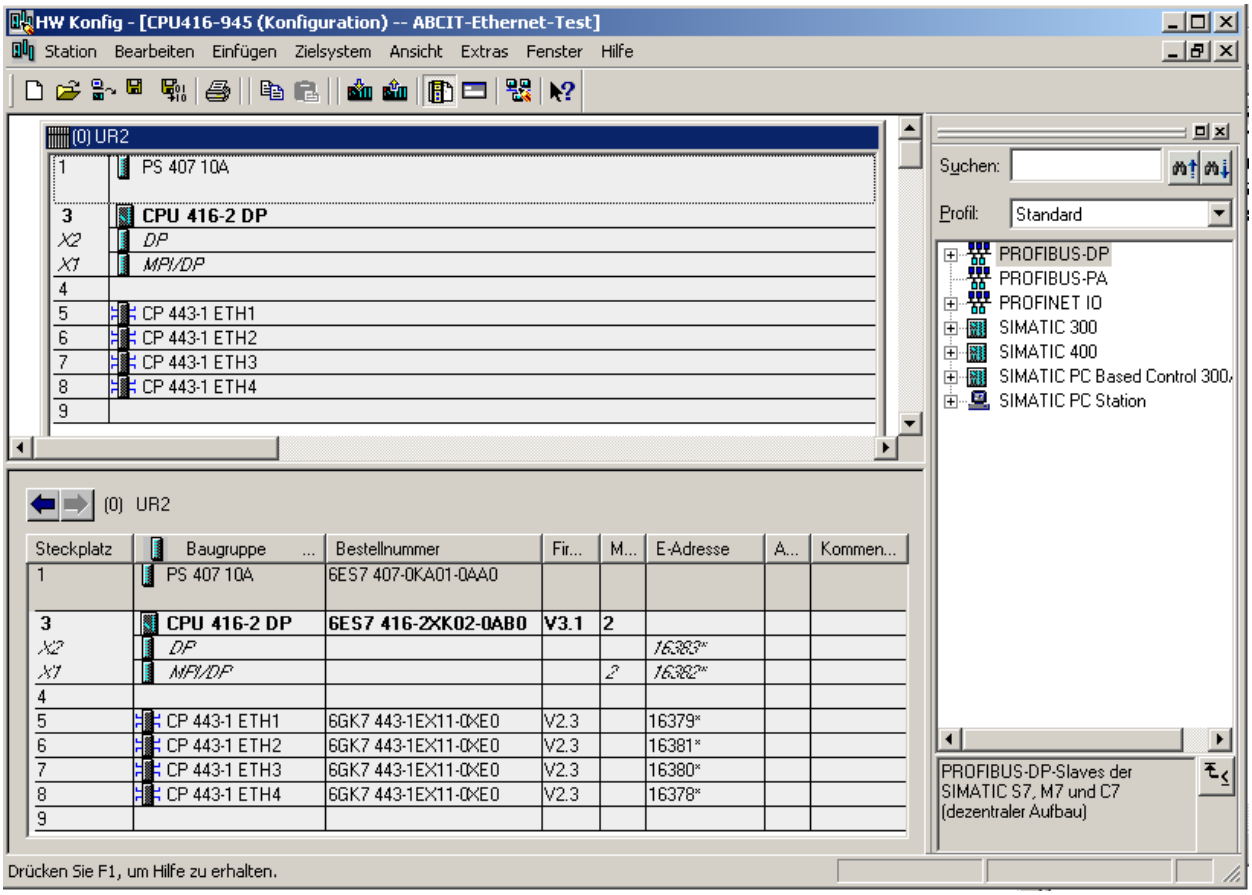
#HW-Config Rack/Slot	
-CPUSlot:3	Slot of the CPU
-CP1Slot:5	Slot of the CP1 (ETH1)
-CP2Slot:6	Slot of the CP2 (ETH2)
-CP3Slot:7	Slot of the CP3 (ETH3)
-CP4Slot:8	Slot of the CP4 (ETH4
#Identification S7-CPU	
-CPUHWIdent:ABC-XCPU 100-1200-xx	
-CPUSWIdent:ABC-RS57 200-1050-13	
-CPUHWVersion:3.2	
-CPUSWVersion:12.3.30	
#Identification CP443-1 ETH1..4	
-CP0HWIdent:ABC-XCPU 100-1200-xx	
-CP0SWIdent:ABC-RS57 200-1050-13	
-CP0HWVersion:3.2	
-CP0SWVersion:12.3.30	
#Ethernet TCP/IP Parameter	
-ETH1Addr:192.168.0.90	IP address of the CP1 after memory reset and STOP→RUN
-ETH1Mask:255.255.255.0	Subnetmask –“”-
-ETH1Rout:0.0.0.0	Router IP adress –“”-
-ETH2Addr:192.168.1.90	IP address of the CP2 after a memory reset and STOP→RUN
-ETH2Mask:255.255.255.0	Subnetmask –“”-
-ETH2Rout:0.0.0.0	Router IP address –“”-
-ETH3Addr:192.168.2.90	IP address of the CP3 after a memory reset and STOP→RUN
-ETH3Mask:255.255.255.0	Subnetmask –“”-
-ETH3Rout:0.0.0.0	Router IP address –“”-
-ETH4Addr:192.168.3.90	IP address of the CP4 after memory reset and STOP→RUN
-ETH4Mask:255.255.255.0	Subnetmask –“”-

-ETH4Rout:0.0.0.0	Router IP address –“”-

1.4.2 HW Konfig (Simatic Manager)

A hardware configuration must be created in the HW configuration of the Simatic Manager. An example configuration is provided in the Samples.zip file. This is a component of the delivery package or you will find it in the download area at the homepage www.abcit.eu.

IMPORTANT!! Please use ABCIT samples as a template. Other configurations can cause problems.



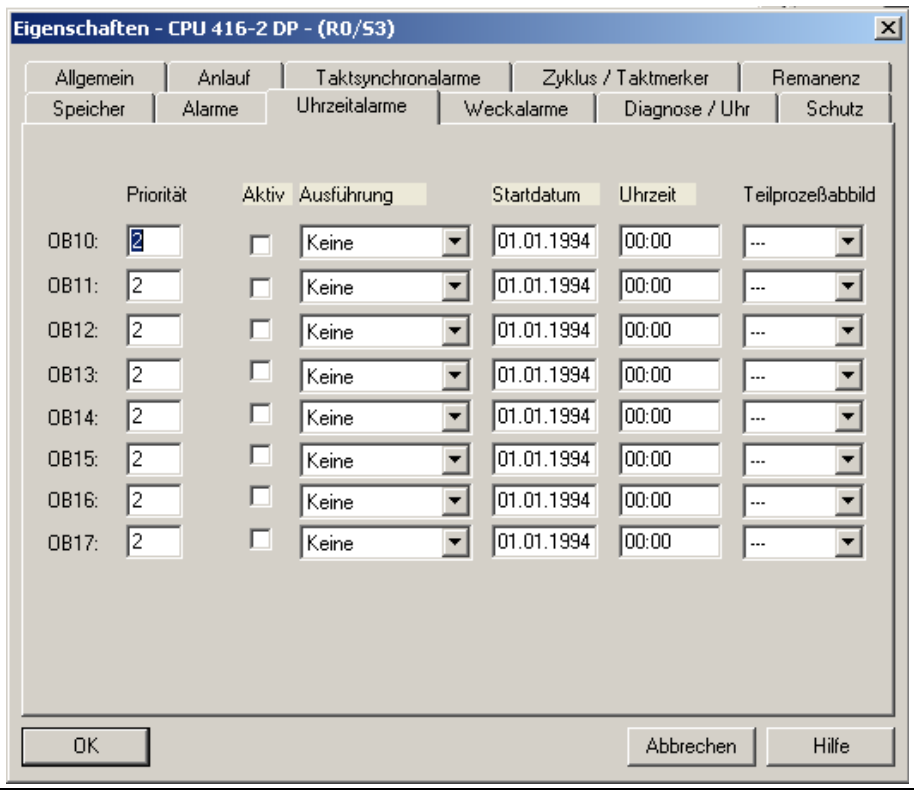
The standard configuration plans that the CPU is plugged into slot 3 and the internal CPs (ETH1…ETH4) as of slot 5.

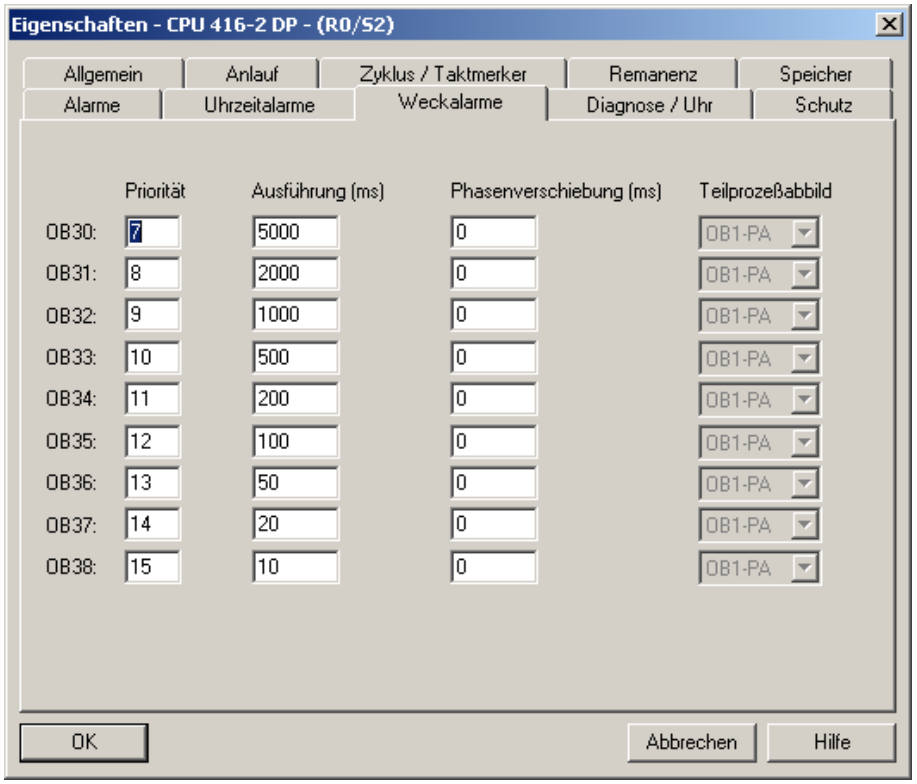
A deviation from the slot positions must be entered in cmdline.txt (on the SD card).

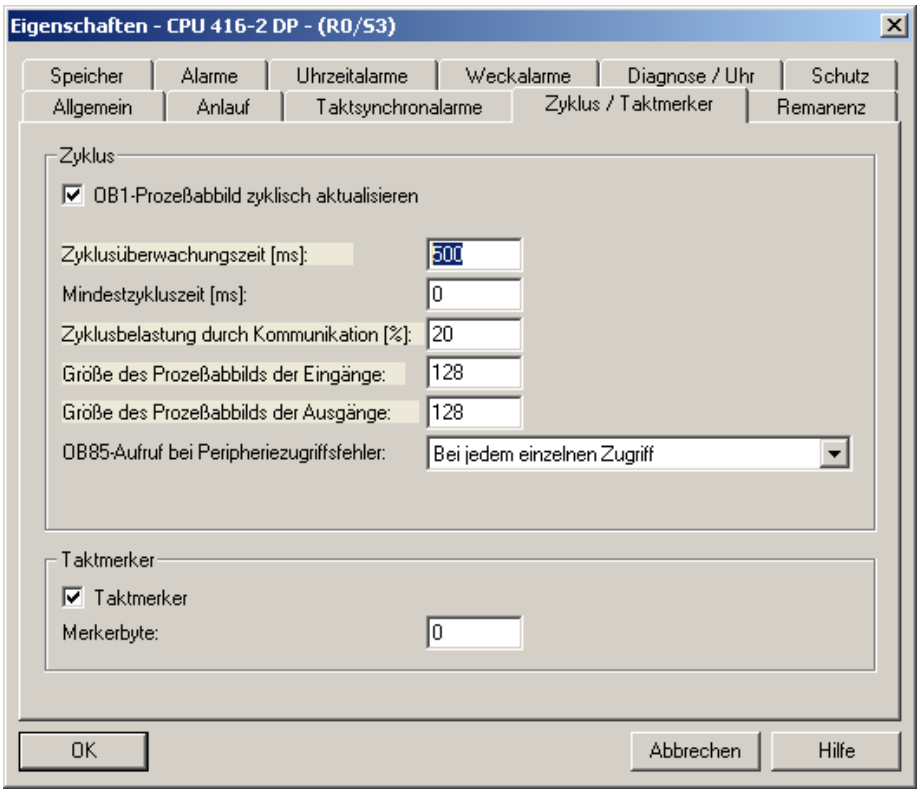
1.4.2.1 CPU 416-2 DP Properties

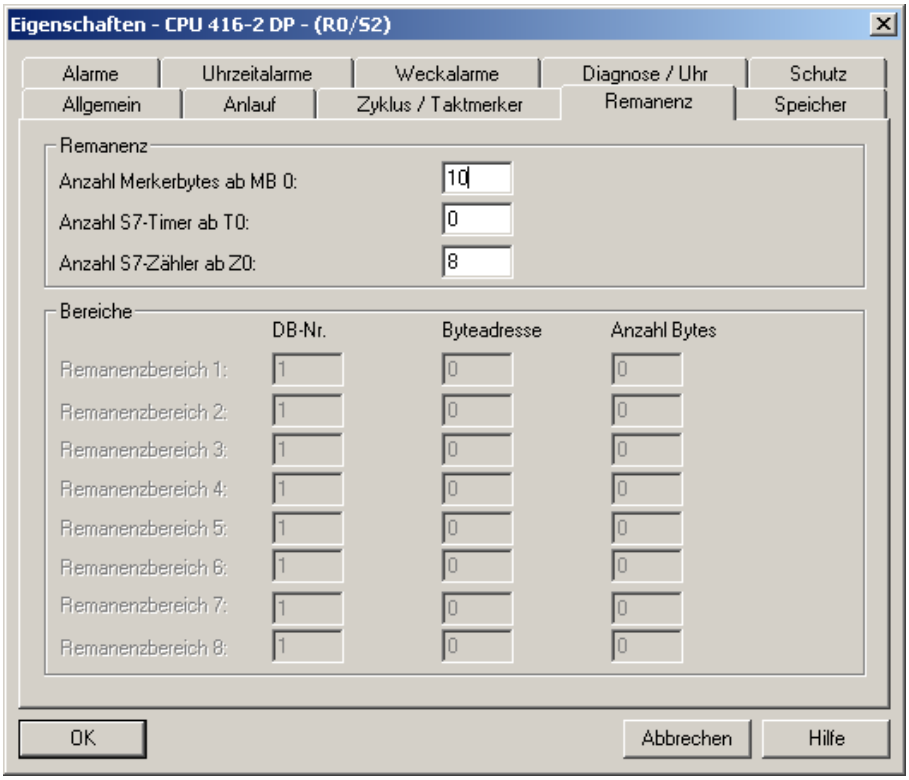
The following parameterizations of the X-CPU-6 can be carried out with the hardware configuration of the Simatic Manager:

Time alarms	
OB10..OB17	Supported parameters: - Priority - Active - Execution - Start date, time of date

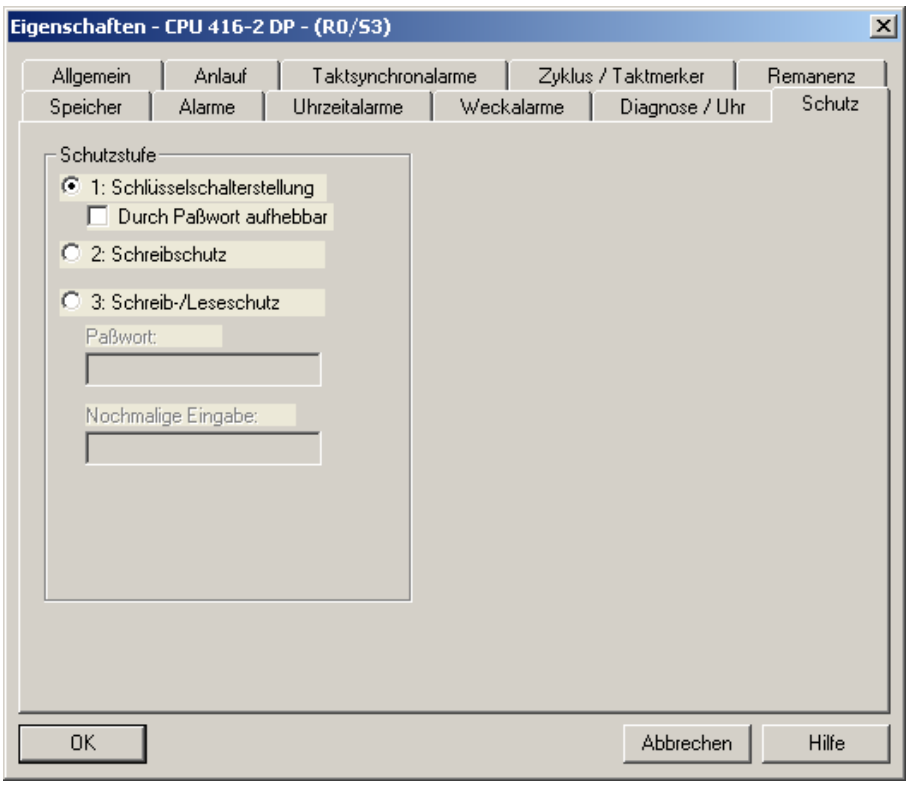


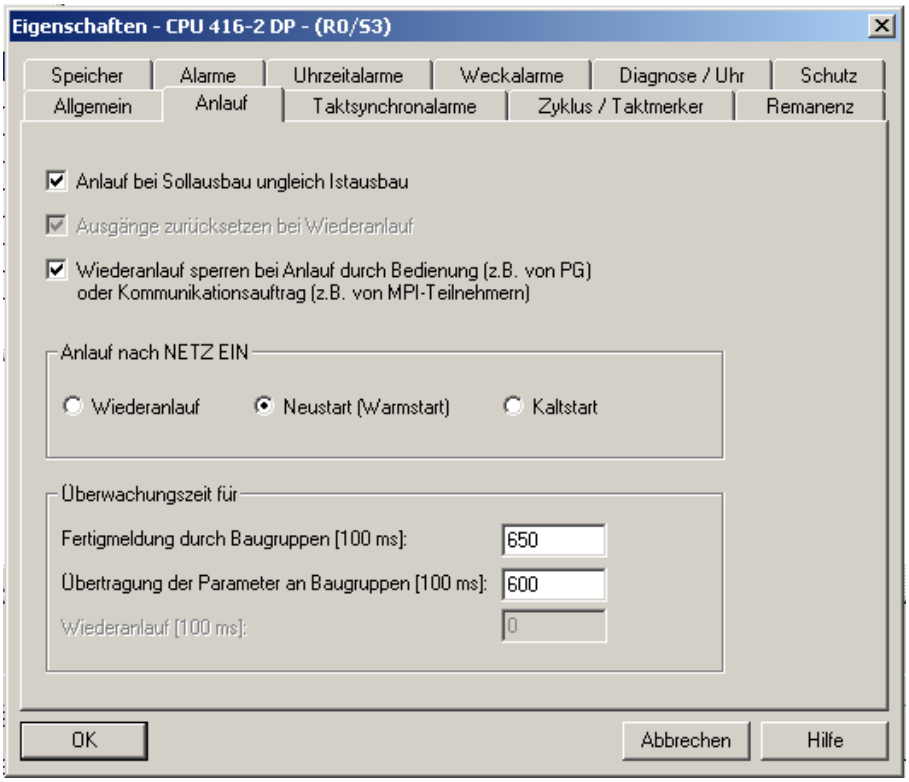
Wake-up alarms	
OB30..OB38	Supported parameters: - Priority - Phase shift - Execution time 

Cycle/tact markers	
Cycle	Supported parameters: - Cyclically update OB1 process image. Here, the number of input/output bytes is indicated that should be cyclically updated starting from 0. **Important!!! In the case of asynchronous balanced mode S7/S5, a max. of 128 may be entered, otherwise QVZ when updating the process image.** The memory size of the process image for inputs and outputs is predefined from 0.0 to 16383.7 respectively. - Cycle monitoring time - Minimum cycle time 
Tact marker	Supported parameters: - Tact marker byte n

Remanence	
Remanence	Supported parameters: - Number of marker bytes as of MB 0: - Number of S5 timers as of T0: - Number of S7 counters as of Z0: 

Protection	
Protection level	Supported parameters: - Write protect - Write/Read protect - Password

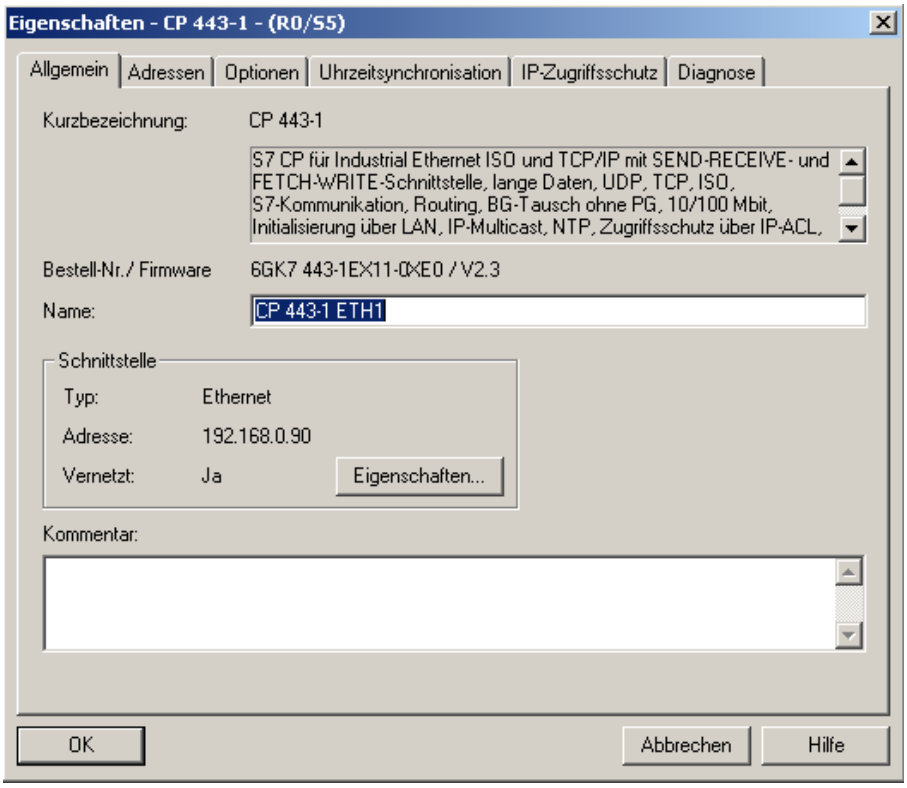

Eigenschaften - CPU 416-2 DP - (R0/S3)
Allgemein
Anlauf
Taktsynchronalarme
Zyklus / Taktmerker
Remanenz
Speicher
Alarme
Uhrzeitalarme
Weckalarme
Diagnose / Uhr
Schutz
Schutzstufe
1: Schlüsselschalterstellung
Durch Paßwort aufhebbar
2: Schreibschutz
3: Schreib-/Leseschutz
Paßwort:
Nochmalige Eingabe:
OK
Abbrechen
Hilfe

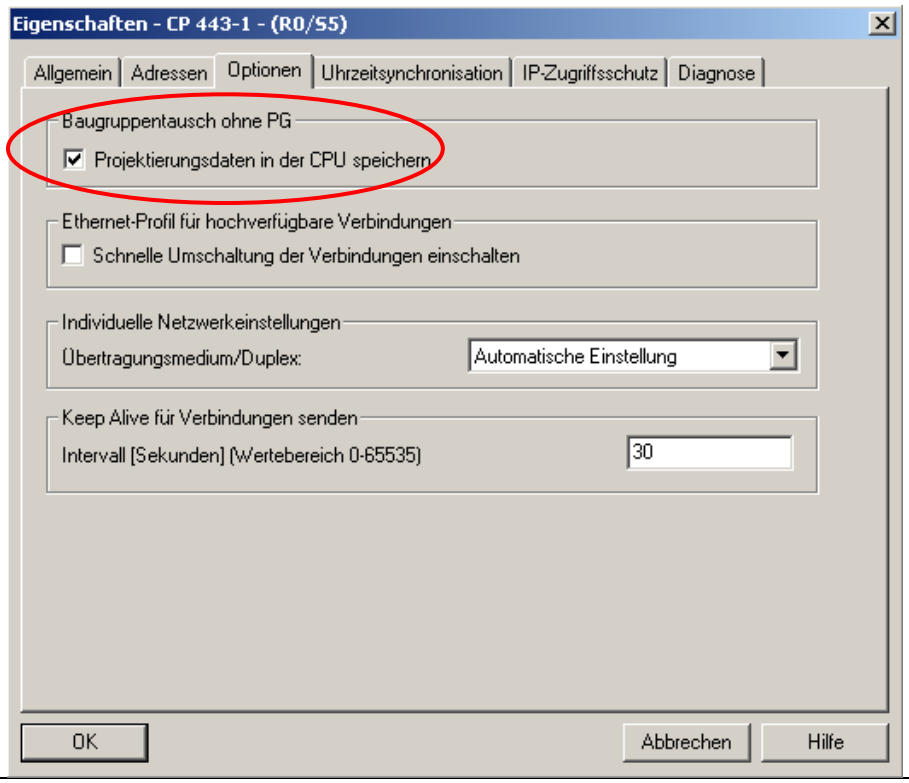
Start-up	
Start-up	Supported parameters: - Recovery, restart (warm start), cold start after NETWORK ON - Completion message through modules - Transfer of parameters to modules - Recovery 

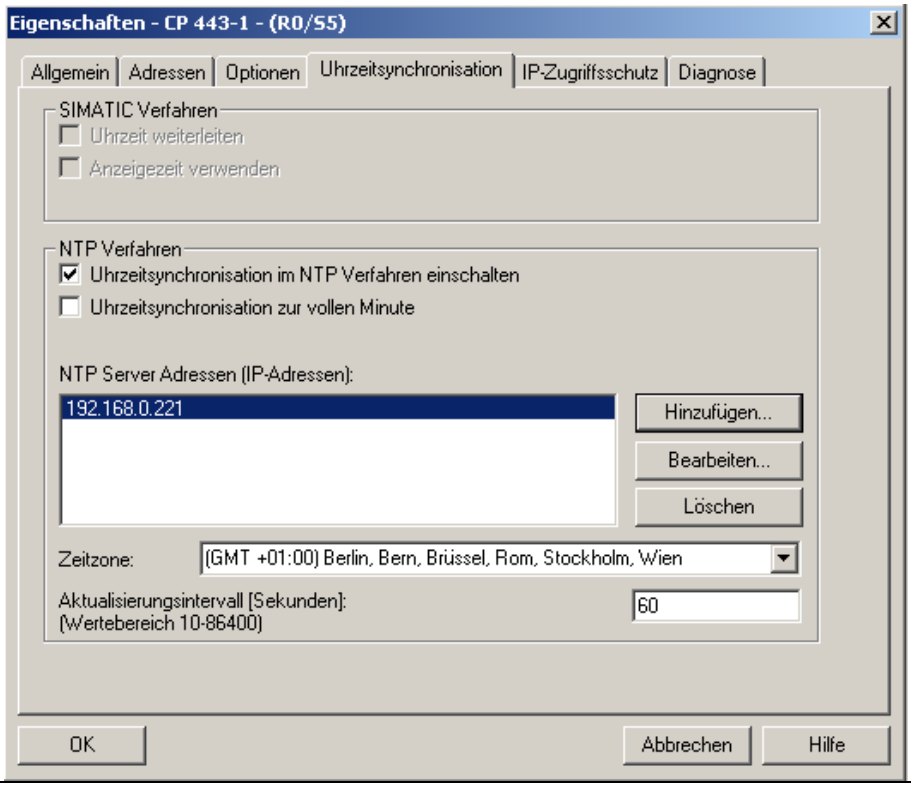
1.4.2.2 CP 443-1 Properties

Important!!! The IP addresses of the four internal CPs must be entered respectively in different sub-networks.

The following parameterisations of the CPs (ETH1…ETH4) can be carried out with the hardware configuration of the Simatic Manager:

General	
	Supported parameter: - Properties (IP address assigned) 

Options	
Planning data	Supported parameter: - Save planning in the CPU. This entry is absolutely necessary. 

Cykle/Takt-marker	
Cycle	Supported parameter: - Switch on time synchronisation in the NTP procedure - Time synchronisation to the full minute - Updating interval - NTP server address 

1.4.3 SYSPARAM-DB

The expanded object properties of the X-CPU-6 CPU416 software that cannot be entered in the HW configuration are summarised in a shared data component.

The data component is structured and is identified by the identifier 'SYSPARAM'.

The SYSPARAM DB can possess any number of data component numbers. Following a restart/cold start, all data components are searched for the identifier. The search takes place sequentially from 1 to N. The first data component with the SYSPARAM identifier parameterises the CPU.

1.4.3.1 System Dependent Parameter

System parameters are used to define and configure the RF7 internal modules.

```
SDP : STRUCT
   TAG:  STRING   [4  ] := 'SDP:';
   RDLY: STRING      [8  ] := 'RDLY 0';
   RF:       STRING       [8  ] := 'RF 32';
   RS:       STRING       [8  ] := 'RF Y';
   RT:       STRING       [8  ] := 'RT 16';
   RC:       STRING       [8  ] := 'RC 8';
   PO:       STRING       [8  ] := 'PO N';
   SW:       STRING       [8  ] := 'SW K';
   INT:  STRING      [8  ] := 'INT O';
   END:  STRING   [1  ] := ';';
END_STRUCT ;
```

System Dependent Parameter (SDP)

RDLY n	RUN-Delay in ms
RF n, Y, N	**Remanent S5 marker** in the asynchronous balanced mode CPU416/945 or CPU416/948 n remanent marker, N no marker remanent, Y 128 marker remanent; No S5 S markers are remanent by default
RS n, Y, N	**Remanent S5 marker** in the asynchronous balanced mode CPU416/945 or CPU416/948 n remanent SMarker, N no SMarker remanent, Y 2048 SMarker remanent No S5 S markers are remanent by default
RT n, Y, N	**Remanent S5 times** in the asynchronous balanced mode CPU416/945 or CPU416/948 n remanent timer, N no timer remanent, Y 64 timer remanent No S5 S markers are remanent by default
RC n, Y, N	**Remanent S5 counters** in asynchronous balanced mode CPU416/945 or CPU416/948 n remanent counter, N no counter remanent, Y 64 counter remanent No S5 S markers are remanent by default
PO H, W, C	Power ON start-up behaviour (recovery H, warm start W, cold start C)

SW W, C	Switch STOP->START start-up behaviour (warm start W, cold start C)
INT O, B	Interruption O=Operations (Default), B=Blocks The 150U mode (INT B) is active in the CPU948 and the mixed variant CPU416_948.

1.4.3.2 Information Technology Parameter

The information parameter are used for configuring the Ethernet TCP/IP module.

```
ITP : STRUCT
 TAG : STRING     [4  ] := 'ITP<0>:';
 INET : STRING    [20 ] := 'INET 0.0.0.0';
 MASK : STRING    [20 ] := 'MASK 0.0.0.0';
 ROUT : STRING    [20 ] := 'ROUT 0.0.0.0';
 DHCP : STRING    [6  ] := 'DHCP N';
 DNS : STRING     [20 ] := 'DNS 0.0.0.0';
 HOST : STRING    [80 ] := 'HOST X7';
 DOM : STRING     [80 ] := 'DOM ABCIT';
 GUI : STRING     [6  ] := 'GUI N';
 END : STRING     [1  ] := ';';
END_STRUCT ;
```

Information Technology Parameter (ITP)

ITP <x>	IP-Adresse des CP x definieren; ETH1==CP0,…ETH4==CP3
INET	IP-Address 192.168.0.90
MASK	Subnet-Mask 255.255.255.0
ROUT	Router Address 192.168.0.1
HTTP	HTTP-Server aktiv J/N
FTP	FTP-Server aktiv J/N
DHCP	DHCP aktiv J/N
DNS	DNS-Server Address 192.168.0.1
HOST	Host-Name “X7”
DOM	Domain-Name ‘ABCIT”
GUI	Graphical User Interface aktiv J/N

1.4.3.3 Extension CIFX

The following entry is required for expansion with an ABC extension.

```
CIFX : STRUCT
   TAG : STRING  [10 ] := 'CIFX<0>:';
   D   : STRING  [6 ]  := 'D DP';
   BF  : STRING  [4 ]  := 'BF Y';
   I   : STRING  [10 ] := 'I 2000 32';
   O   : STRING  [10 ] := 'O 2000 32';
   PII : STRING  [12 ] := 'PII 2000 32';
   PIO : STRING  [12 ] := 'PIO 2000 32';
   END : STRING  [1 ] := ';';
 END_STRUCT ;
```

CIFX<0>	*Extensionboard*
D XX	Device DP=Profibus, PN=Profinet, EC=EtherCAT
BF N/Y	Bus-Fault Y/N
I x y	Input from offset x length y Byte
O x..y	Output from offset x length y Byte
PII x y	Process Image Inputs from offset x length y Byte
PIO x y	Process Image Output from offset x length y Byte

1.4.3.4 Hardware process alarm

```
INTX : STRUCT
   TAG : STRING  [10 ] := 'INTX:';
   INTA: STRING  [10 ] := 'INTA Y';
   INTE: STRING  [10 ] := 'INTE N';
   INTF: STRING  [10 ] := 'INTD N';
   INTG: STRING  [10 ] := 'INTG N';
   END : STRING  [1 ] := ';';
 END_STRUCT ;
```

INTX	
INTA-D, E, F, G	The hardware process alarms depend upon the slot. A-D are represented by the CPU slots 1-4 in a 135/155 system.
N/Y	INTA → OB40, INTE → OB41, INTF → OB42, INTG → OB43 Attention: the EB0-PRAL must be deactivated when INTX is active.

1.4.3.5 Process alarm EB0

```
PRAL : STRUCT
   TAG : STRING  [10 ] := 'PRAL:';
   EB0 : STRING  [10 ] := 'EB0 Y';
   END : STRING  [1 ] := ';';
 END_STRUCT ;
```

PRAL	
EB0 Y/N	EB0 Y/N The EB0 process alarm recognises flank changes on the EB0 and triggers the accordingly assigned OBs: EB 0.0 → OB40... EB 0.7 → OB47 Attention: the INTX must be deactivated when EB0-PRAL is active.